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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/702,235	11/05/2003	Peter C. Salmon	A-70884-1/AJT	7939

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EXAMINER	
HARRISON, MONICA D	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/702,235	SALMON, PETER C.	
	Examiner	Art Unit	
	Monica D. Harrison	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) *1-18,30-36,42,43 and 46-50* is/are withdrawn from consideration.

5)☒ Claim(s) *40,41,44 and 45* is/are allowed.

6)☒ Claim(s) *19-29 and 37-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 1-18, 30-36, 42, 43 and 46-50 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Group I, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 8/3/05.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 19-24, 26, 27, 29 and 38 are rejected under 35 U.S.C. 102(e) as being anticipated by Bertin et al (6,141,245).

2. Regarding claim 19, Bertin et al discloses a method for fabricating an electronic circuit comprising the steps of: providing a rigid carrier (Figure 4A, reference 102); applying a base dielectric layer on said rigid carrier (Figure 4A, reference 104); fabricating one or more interconnection circuits having exposed input/output pads on said base layer (Figure 2A, reference 75a); fabricating wells at said input/output pads of said interconnection circuits (Figure 6A); and filling said wells with conductive material (Figure 6A, reference 148).

3. Regarding claim 20, Bertin et al discloses including the additional step of attaching electronic components to said interconnection circuits to form an electronic assembly, wherein each of said components has a conductive bump at each of its input/output pads, and each of said conductive bumps is inserted into said conductive material in one of said wells (Figure 5B, reference 96).

4. Regarding claim 21, Bertin et al discloses including the step of fabricating a release layer interposed between said rigid carrier and said base dielectric layer (Figure 4B, reference 122).

5. Regarding claim 22, Bertin et al discloses separating said interconnection circuit or electronic assembly from said rigid carrier at said release layer, after completing said circuit or assembly (Figure 9A).

6. Regarding claim 23, Bertin et al discloses wherein said interconnection circuits comprise multiple dielectric and conducting layers (column 6, lines 65-66).

7. Regarding claim 24, Bertin et al discloses wherein said dielectric layers are polymer layers that are patterned using light projected through a mask (Figure 4A, reference 112).

8. Regarding claim 26, Bertin et al discloses wherein said release layer is not present near the edges of said rigid carrier, to provide an edge region of strong adhesion between said base dielectric layer and said rigid carrier (Figure 4B, reference 122).

9. Regarding claim 27, Bertin et al discloses wherein said release layer is additionally not present in streets at the periphery of a plurality of said interconnection circuits (Figure 4B, reference 122).

10. Regarding claim 29, Bertin et al discloses wherein said wells are formed with essentially vertical walls (Figure 6A (3)).

11. Regarding claim 38, Bertin et al discloses a method for forming wells filled with conductive material on an interconnect circuit comprising the steps of: applying a layer of dielectric material on top of said interconnect circuit (Figure 4A, reference 104); forming openings in said dielectric layer at each input/output pad of said interconnect circuit (Figure 4A, reference 111); and depositing said conductive material in said openings to form wells filled with conductive circuit (Figure 4B, reference 130; Figure 6A, *wells*).

Claim 37 is rejected under 35 U.S.C. 102(e) as being anticipated by Hedler et al (6,664,176 B2).

12. Hedler et al discloses a trace routing method for a multi-layer interconnection circuit comprising the steps of: providing stacked contacts with lace stubs at input/output pads of said interconnection circuit; and limiting contacts between conductive layers to two-level contacts in routing areas where maximum routing density is desired (Figure 7).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bertin et al (6,141,245) in view of Towle et al (6,846,737 B1).

13. Bertin discloses all above claimed subject matter except the release layer is a fluorinated silicone (claim 25).

Towle et al discloses a fluorinated silicone polymer (column 8, line 27; claim 18).

Since Bertin et al and Towle et al are both from the same field of endeavor, the purpose disclosed Towle et al would have been recognized in the pertinent art of Bertin et al.

It is obvious at the time the invention was made, for one with ordinary skill in the art, to modify Bertin et al with the teachings of Towle et al for the purpose of providing a fluorine concentration in an insulator suitable for use in integrated circuits.

Claims 28 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bertin et al (6,141,245) in view of Hedler et al (6,664,176).

14. Bertin et al discloses the above independent claimed subject matter of claims 19 and 38 however, Bertin et al does not disclose the squeegee (claims 28 and 39).

Hedler et al discloses the squeegee (column 6, lines 50-54).

Since Bertin et al and Hedler et al are both from the same field of endeavor, the purpose disclosed by Hedler et al would have been recognized in the pertinent art of Bertin et al.

It is obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Bertin et al with the teachings of Hedler et al for the purpose of distributing conductive polymers directly onto a circuit in order to minimize placement error within circuit patterns.

Allowable Subject Matter

15. Claims 40, 41, 44 and 45 are allowed over the prior art of record.

Reasons for Allowance

16. The following is an examiner's statement of reasons for allowance: The primary reason for allowance of the claims is that the prior art neither teaches nor fairly suggest a method for assembling integrated circuit chip that inserts conductive bumps into wells filled with solder in claims 40 and 41 and in the context of the recited process.

The primary reason for allowance of the claims is that the prior art neither teaches nor fairly suggest a method for reworking defective components mounted on a circuit substrate that withdraw defective components from wells; clean the area surrounding the well, then adding solder to said wells in order to replace conductive bumps of a replacement component in claims 44 and 45 and in the context of the recited process.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is 571-272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Monica D. Harrison
AU 2813

mdh
September 29, 2005

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